UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/694,477	10/27/2003	Shunpei Yamazaki	0553-0118.01	4264

7590 05/18/2007

Edward D. Manzo
Cook, Alex, McFarron, Manzo,
Cummings & Mehler, Ltd.
200 West Adams St., Ste. 2850
Chicago, IL 60606

EXAMINER	
PRENTY, MARK V	
ART UNIT	PAPER NUMBER
2822	

MAIL DATE	DELIVERY MODE
05/18/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/694,477	YAMAZAKI, SHUNPEI	
	Examiner	Art Unit	
	MARK PRENTY	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 May 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *24,25,28-30,33-35,38,39,41,43,44,46,48,49,51,53-65 and 69-87* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *39,41,43,44,46,48,49,51,53,57-65 and 69-83* is/are allowed.

6)☒ Claim(s) *24,25,28-30,33-35,38,54-56,84,86 and 87* is/are rejected.

7)☒ Claim(s) *85* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

This Office Action is in response to the amendment filed May 1, 2007.

Claims 24, 25, 28, 54, 84, 86 and 87 are rejected under 35 U.S.C. 103(a) as being unpatentable over United States Patent 5,455,791 to Zaleski et al. (Zaleski, already of record) together with United States Patent 5,488,001 to Brotherton.

As to independent claim 24, Zaleski discloses a semiconductor device (see the entire patent, including the Fig. 1 disclosure) comprising: a semiconductor film 2b; a pair of first impurity regions 4a, 4b being formed in the semiconductor film; an active region 4c formed between the pair of first impurity regions in the semiconductor film; a floating gate 6 formed over and insulated from the active region; and a control gate 8 formed over and insulated from the floating gate.

The difference between claim 24 and Zaleski is claim 24 further comprises: "at least two second impurity regions formed in said semiconductor film between the pair of first impurity regions; at least one channel region between the at least two second impurity regions; boundaries between the channel region and the at least two second impurity regions extend in a direction along a carrier flow direction of the channel region...wherein the floating gate overlaps a boundary between at least one of the pair of the first impurity regions and the at least two second impurity regions."

Brotherton teaches providing a thin film transistor with two second impurity regions extending from the source region to the drain region to reduce leakage current (see the entire patent, including the Fig. 6 disclosure).

It would have been obvious to one skilled in this art to provide Zaleski's thin film transistor with two second impurity regions extending from source region 4b to drain

region 4a (resulting in a semiconductor device whose floating gate overlaps a boundary between at least one of the pair of the first impurity regions and the two second impurity regions) to reduce leakage current as taught by Brotherton.

Claim 24 is thus rejected under 35 U.S.C. 103(a) as being unpatentable over Zaleski together with Brotherton.

As to dependent claim 25, Brotherton teaches that its second impurity regions 5 preferably have a striped shape.

Claim 25 is thus rejected under 35 U.S.C. 103(a) as being unpatentable over Zaleski together with Brotherton.

As to dependent claim 28, Brotherton also teaches that thin film semiconductor devices are conventionally used in electronic devices (see column 1, first full paragraph). It would have been further obvious to one skilled in the art to use the obvious Zaleski/Brotherton semiconductor device in an electronic device because Brotherton further teaches that thin film semiconductor devices are conventionally used in electronic devices.

Claim 28 is thus rejected under 35 U.S.C. 103(a) as being unpatentable over Zaleski together with Brotherton.

As to dependent claim 54, Zaleski's device further comprises an insulating layer 3 that underlies semiconductor film 2b, and Brotherton further teaches providing such an insulating layer with the same conductivity type impurity element as the two second impurity regions to reduce leakage current (see column 6, lines 23-28).

Claim 54 is thus rejected under 35 U.S.C. 103(a) as being unpatentable over Zaleski together with Brotherton.

As to independent claim 84, Zaleski discloses a semiconductor device (see the entire patent, including the Fig. 1 disclosure) comprising: an oxide film 3; a semiconductor film 2b formed over the oxide film, including a source region 4b, a channel forming region 4c, and a drain region 4a; a floating gate 6 formed over the channel forming region with a gate insulating film 5 interposed therebetween; and a control gate 8 formed over the floating gate.

The difference between claim 84 and Zaleski is claim 84 further comprises a pair of impurity regions formed at side edges along the channel length direction, and a portion of claim 84's oxide film has the same conductivity type as that of the pair of impurity regions.

Brotherton teaches providing a thin film transistor with a pair of impurity regions formed at side edges along the channel length direction to reduce leakage current (see the entire patent, including the Fig. 6 disclosure). Brotherton also teaches making a portion of the insulating layer under the thin film the same conductivity type as that of the pair of impurity regions to reduce leakage current (see column 6, lines 23-28).

It would have been obvious to one skilled in this art to provide Zaleski's thin film transistor with a pair of impurity regions formed at side edges along the channel length direction and to make a portion of the insulating layer 3 under the thin film the same conductivity type as that of the pair of impurity regions to reduce leakage current as taught by Brotherton.

Claim 84 is thus rejected under 35 U.S.C. 103(a) as being unpatentable over Zaleski together with Brotherton.

As to dependent claim 86, Brotherton's pair of impurity regions 5 is opposite conductivity type to the source and drain regions.

Claim 86 is thus rejected under 35 U.S.C. 103(a) as being unpatentable over Zaleski together with Brotherton.

As to dependent claim 87, Zaleski's semiconductor film 2b is a single crystal silicon film.

Claim 87 is thus rejected under 35 U.S.C. 103(a) as being unpatentable over Zaleski together with Brotherton.

Claims 29, 30, 33-35, 38, 55 and 56 are rejected under 35 U.S.C. 103(a) as being unpatentable over United States Patent 5,455,791 to Zaleski et al. (Zaleski, already of record) together with United States Patent 5,488,001 to Brotherton and United States Patent 5,814,854 to Liu et al (Liu, already of record).

Independent claim 29 parallels independent claim 24 except that claim 29 further recites a NOR type circuit comprising a plurality of transistors. The explanation of the above rejection of claim 24 under 35 U.S.C. 103(a) as being unpatentable over Zaleski together with Brotherton is thus hereby incorporated by reference into this rejection of claim 29 under 35 U.S.C. 103(a) as being unpatentable over Zaleski together with Brotherton and Liu.

The difference, therefore, between independent claim 29 and the obvious Zaleski/Brotherton device is claim 29 recites a NOR type circuit.

Liu, however, teaches that EEPROM devices are conventionally used to form NOR type circuits (see column 4, lines 1-16).

It would have been further obvious to one skilled in the art use the obvious Zaleski/Brotherton EEPROM device in a NOR type circuit because Liu teaches that EEPROM devices are conventionally used to form a NOR type circuit.

Claim 29 is thus rejected under 35 U.S.C. 103(a) as being unpatentable over Zaleski together with Brotherton and Liu.

Independent claim 29's dependent claims 30 and 33 parallel independent claim 24's dependent claims 25 and 28 (addressed above) and are thus also rejected under 35 U.S.C. 103(a) as being unpatentable over Zaleski together with Brotherton and Liu.

Independent claim 34 parallels independent claim 24 except that claim 34 further recites a NAND type circuit comprising a plurality of transistors. The explanation of the above rejection of claim 24 under 35 U.S.C. 103(a) as being unpatentable over Zaleski together with Brotherton is thus hereby incorporated by reference into this rejection of claim 34 under 35 U.S.C. 103(a) as being unpatentable over Zaleski together with Brotherton and Liu.

The difference, therefore, between independent claim 34 and the obvious Zaleski/Brotherton device is claim 34 recites a NAND type circuit.

Liu, however, teaches that EEPROM devices are conventionally used to form NAND type circuits (see column 4, lines 1-16).

It would have been further obvious to one skilled in the art use the obvious Zaleski/Brotherton EEPROM device in a NAND type circuit because Liu teaches that EEPROM devices are conventionally used to form a NAND type circuit.

Claim 34 is thus rejected under 35 U.S.C. 103(a) as being unpatentable over Zaleski together with Brotherton and Liu.

Independent claim 34's dependent claims 35 and 38 parallel independent claim 24's dependent claims 25 and 28 (addressed above) and are thus also rejected under 35 U.S.C. 103(a) as being unpatentable over Zaleski together with Brotherton and Liu.

As to dependent claims 55 and 56, Zaleski's device further comprises an insulating layer 3 that underlies semiconductor film 2b, and Brotherton further teaches that such an insulating layer should comprise the same conductivity type impurity element as the two second impurity regions to reduce leakage current (see column 6, lines 23-28).

Claims 55 and 56 are thus rejected under 35 U.S.C. 103(a) as being unpatentable over Zaleski together with Brotherton and Liu.

Claim 85 is objected to as being dependent upon a rejected base claim, but would be allowable over the prior art of record if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 39, 41, 43, 44, 46, 48, 49, 51, 53, 57-65 and 69-83 are allowable over the prior art of record.

Registered practitioners can telephone the examiner at (571) 272-1843. Any voicemail message left for the examiner must include the name and registration number of the registered practitioner calling, and the Application/Control (Serial) Number. Technology Center 2800's general telephone number is (571) 272-2800.

Mark Prenty

Mark V. Prenty
Primary Examiner